DSTD-777

HIGH RESOLUTION GRAPHICS CONTROLLER OPERATIONS MANUAL

PREPARED BY: dy-4 SYSTEMS INC.
DATED: OCTOBER 24, 1983

DY-4 SYSTEMS INC., 888 LADY ELLEN PLACE, OTTAWA, ONTARIO, CANADA K1Z 5M1 (613) 728-3711

TABLE OF CONTENTS

APPENDICES

LIST OF TABLES

LIST OF FIGURES

Acknowledgements

SECTION 1

1.0 GENERAL INFORMATION

1.1 Introduction

The DSTD-777 is a high resolution graphics controller card. It is produced in two forms. The DSTD-777A supports the color mode with a dot resolution of up to 640 by 480 interlaced. In color mode the card will also support an eight level monochromatic display format. The DSTD-777B supports the monochromatic mode with a dot resolution of up to 1024 by 768 interlaced. The DSTD-777 is designed around the powerful NEC-7220 graphics processor chip which performs high level graphic operations such as vector drawing, arcs and circles, rectangular drawing and rectangular fill.

1.2 DSTD Series General Description

The dy-4 DSTD Series of STD-BUS compatible products was designed to satisfy the need for high performance microcomputer modules that could be quickly and inexpensively integrated into a variety of end-user applications. The popular STD-BUS motherboard interconnect system concept provides expandability as needs change. Support by numerous manufacturers provides the user with a choice from scores of compatible products.

The modules are a compact 4.5 x 6.5 inches (11.4 X 16.5 cm) which provides for system partitioning by function, i.e. CPU, Memory, I/O, etc. dy-4 SYSTEMS has been able to combine most popular functions on single cards to reduce system card count and cost.

1.3 DSTD-777 Features

* 640 by 480 interlaced color dot resolution (DSTD-777A).
* 1024 by 768 interlaced monochromatic dot resolution. (DSTD-777B)
* Powerful NEC-7220 graphics processor chip
* Separate sync, composite sync or composite sync on green options
* Supports TTL Light Pen
* NEC 7220 DMA operation supported in both hardware and software modes
* External sync option

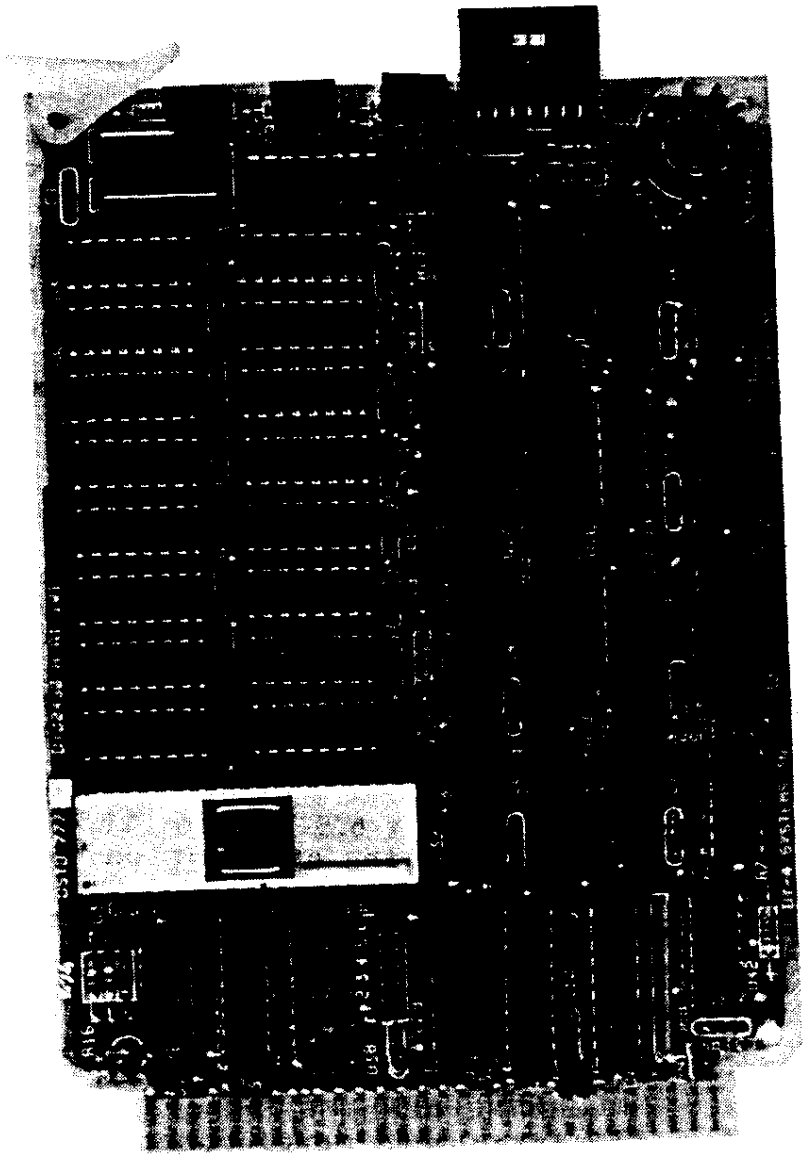


FIGURE 1 - 1

DSTD-777 HIGH RESOLUTION GRAPHICS CONTROLLER

SECTION 2

2.0 FUNCTIONAL DESCRIPTION

2.1 Introduction

The DSTD-777 is a high resolution graphics controller card designed to handle both monochromatic and color modes of operation. The card is designed to handle two display formats. The DSTD-777A supports both color and eight level monochromatic formats with a dot resolution of up to 640 by 480 interlaced. The DSTD-777B supports high resolution monochromatic formats with a dot resolution of up to 1024 by 768 interlaced.

The mode of operation is selected by installing the appropriate pixel clock oscillator, option jumpers and PAL micro code sequencer decoder chip set which determines the way the on-board memory is accessed.

The DSTD-777 is designed around the powerful NEC-7220 graphics processor chip.

2.2 Block Diagram Description

The block diagram for the DSTD-777 is shown in figure 2 - 1. The following paragraphs discuss the functions of the various blocks.

2.2.1 STD BUS Interface

The interface logic includes all the buffers for the address, data and control signals, ensuring that the card represents only one TTL load to the bus.

2.2.2 Video Clock Generator

The DSTD-777 derives its timing from one of two sources, on-board by a crystal controlled oscillator or some external device.

In the external mode of operation the pixel clock and VSYNC (the monitor's vertical sync signal) are supplied from an external device. This mode is used when combining two video signals. The VSYNC signal, in this mode, is used by the VDC to synchronize its timing to the external device.

In both cases the pixel clock is divided down to form intermediate timing signals and the word clock which is used to control the loading of the output shift registers and by the NEC chip to generate the monitor Hsync signal.

The pixel clock frequency is selected, taking into account the operation of the NEC-7220 controller, to give the desired display format. Having selected the clock freqency the NEC-7220 is then programmed to get the required Horizontal sync waveforms and, in internal mode, the required Vertical sync waveforms.

The standard clock frequency for a 1024 by 768 monochromatic display is 31.22MHz. The standard clock frequency for a 640 by 480 color or monochromatic display is 14.318MHz

Consult the factory for information on non-standard display format timing.

2.2.3 NEC-7220 Graphics Controller

The DSTD-777 is designed around the NEC-7220 graphics display controller. The GDC supplies the sync signals required by the video monitor (HSYNC and VSYNC), video memory addresses, video blanking and some memory control signals used to read and write data into the display RAM.

On power-up or following a system reset the display is automatically blanked. The GDC is initialized by the microprocessor. The display is then enabled by reading any of the GDC registers. The GDC can now accept high level commands from the microprocessor and perform the commmands returning status or data depending on the command.

The GDC also supports a light pen input.

For a detailed explanation of the GDC refer to the NEC-7220 Programming Guide Handbook available from the factory. Section 4 of this manual includes some programming examples for the standard display formats.

2.2.4 Display Ram and Output Registers

The DSTD-777 has 128 kilobytes of display memory arranged to feed three sets of output shift registers in color and eight level monochrome mode or one set of registers in high resolution monochromatic mode. The shift register control signals are generated by a micro-coded sequencer.

2.2.5 Video Output Drivers

The output of the video shift registers feed three high speed, high current drivers. The drivers are powered by an "analog" power supply derived on-board from the +12 supply. This analog power supply provides a clean video signal.

The video output driver circuitry supports the three display formats:

1) color with three separate drivers (Red, Blue and Green)

2) eight level monochrome with the three drivers combined into one video output.

3) two level (on/off) high resolution where only one video driver is used.

Jumper blocks JB2 and JB3 are used to configure the output stage (refer to Section 3.4). The output stage also includes three potentiometers to set and fine tune the display.

The video output circuitry also allows a composite sync signal to be mixed into one of the outputs. In color mode this output is typically the 'green' gun, thus providng the 'sync on green' option.

Table 2-1 shows the pinout for the video output cable connector.

TABLE 2 - 1

Video Output Connector J2

Pin Number	Description
1	Ground
2	Output Driver, High Res. output or Green
3	Ground
4	Composite Sync or Horizontal Sync
5	Ground
6	Vertical Sync Input or Output
7	Ground
8	Output Driver 2 Blue
9	Ground
10	Output Driver 3 Red
11	Ground
12	External Pixel Clock
13	+5
14	Light Pen Input (TTL)

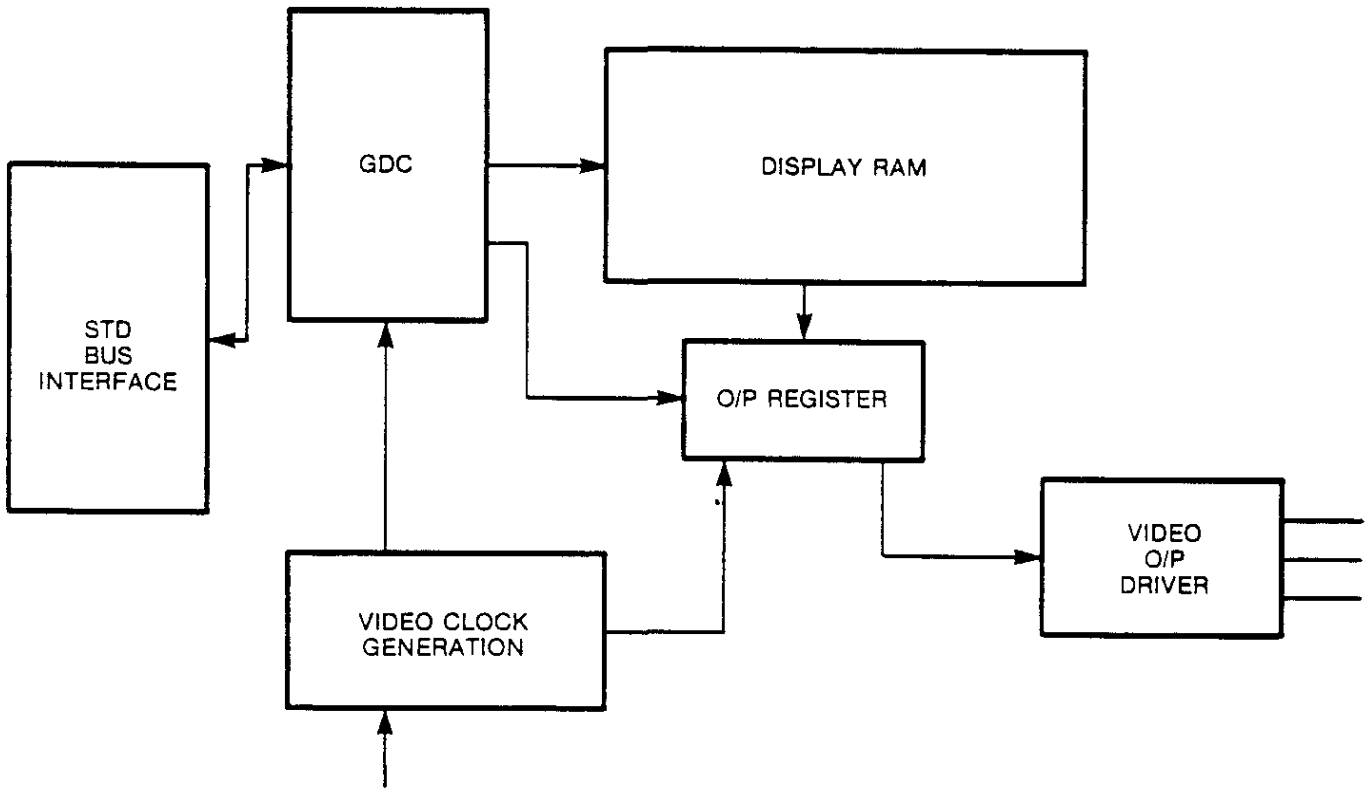


FIGURE 2 - 1

DSTD-777 BLOCK DIAGRAM

SECTION 3

3.0 USER SELECTABLE OPTIONS

3.1 Introduction

The following sections discuss the user selectable or user programmable options. This manual concentrates on the hardware selectable options with only a brief discussion of the system and software options.

3.2 Display Mode Selection

The DSTD-777 can be operated in one of two display modes, namely monochromatic mode or color and eight level mode. The mode is selected by installing the appropriate micro sequencer PALs (U40 and U41) and by setting up jumper block JB7.

Use the PAL set labelled"490xxxA" and install a jumper between JB7-1 and JB7-2 for color or eight level monochromatic operation (640 x 480).

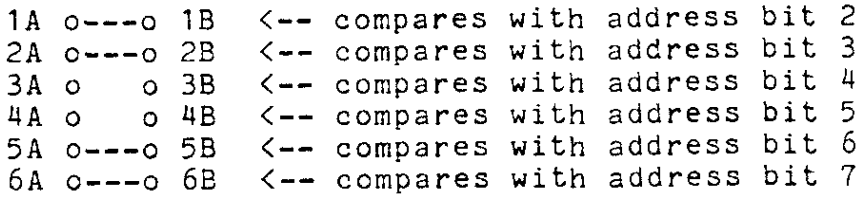
Use the PAL set labelled "490xxxB" and install a jumper between JB7-2 and JB7-3 for monochromatic operation (1024 x 768).

3.3 Card Address Selection (JB1)

The DSTD-777 occupies 4 I/O ports. These I/O ports are positioned using Jumper Block JB1. Shunting adjacent pins creates a low logic level (a '0'), leaving a pair open creates a high logic level (a '1'). These bit values are compared with the lower 8 bits of the address bus. When the two match, the card control registers may be written to and read from. An example is shown in Table 3-1.

TABLE 3 - 1

Card Address Selection JB1



OPEN = '1'
SHORTED = '0'
FACTORY SETTING = 30H, as shown

3.4 Output Driver Configuration

The video output drivers are configured using JB2 and JB3 (refer to the schematic in Appendix D of this manual). There are three basic configurations.

1) color with three separate drivers (Red, Blue and Green)

2) eight level monochrome with the three drivers combined into one video output.

3) two level (on/off) high resolution where only one video driver is used.

The output driver circuitry also includes a transistor connected in an emitter follower configuration for adding the signals and driving output 1.

3.4.1 Color

In color mode the three output drivers are used. The jumpering depends on whether the "composite sync on green" option is required.

Separate Sync	Composite Sync on Green
JB3-2 to JB3-1	JB3-2 to JB3-3
	JB2-3A to JB2-3B
	JB2-4A to JB2-4B

The output levels are adjusted using the three potentiometers R4, R8 and R12

R4	Green
R8	Blue
R12	Red

3.4.2 Eight Level Monochrome

In eight level monochromatic mode the three output drivers are used. The jumpering depends on whether the "composite sync" option is required.

Separate Sync	Composite Sync
JB2-1A to JB2-1B	JB2-1A to JB2-1B
JB2-2A to JB2-2B	JB2-2A to JB2-2B
JB3-2 to JB3-3	JB3-2 to JB3-3
JB2-3A to JB2-3B	JB2-3A to JB2-3B
	JB2-4A to JB2-4B

The output levels are adjusted using the three potentiometers R4, R8 and R12 to give the desired gray levels

R4	Half Tone
R8	Quarter Tone
R12	Eighth Tone

3.4.3 High Resolution Monochrome

In high resolution monochrome mode only one of the three output drivers is used, driver 1. The jumpering depends on whether the "composite sync" option is required.

Separate Sync	Composite Sync
JB3-2 to JB3-1	JB3-2 to JB3-3
	JB2-3A to JB2-3B
	JB2-4A to JB2-4B

The potentiometer R4 can be used to adjust the video output level.

3.5 Video Sync Modes

The DSTD-777 supports several video sync options including an external sync option which allows the video output of the board to be combined with other video sources.

In the external or slave mode the DSTD-777 receives its pixel clock and a TTL Vertical Sync signal from the external device. The pixel clock is used to generate the cards basic timing and the Vertical Sync signal is used by GDC to "lock" to the external device's video sync. To select external or slave mode remove jumper JB4 and install a jumper between JB6-2 and JB6-1.

In internal or master mode, the DSTD-777 derives its pixel clock from an on-board crystal controlled oscillator and the GDC generates its own Horizontal Sync and Vertical Sync signals. To select internal or master mode install JB4 and connect JB6-2 to JB6-3.

Also within the master mode it is possible to select composite sync (horizontal and vertical sync signals are OR'd together) or separate sync modes. This is done using JB5. JB5 is installed to select composite sync mode and not installed to select separate sync mode.

3.6 DMA Mode

The DSTD-777 provides the option to use an external DMA controller to increase the transfer rate of data to and from the VDC chip. This feature is typically used with the DSTD-711 (Floppy Disk Controller with 64 kilobyte of RAM). Both the DSTD-777 and the DSTD-711 are designed to allow the DRQ line of the VDC to be connected to the RDY line of the DMA chip on the DSTD-711 such that the DMA chip on the DSTD-711 can be used to control data transfers to the VDC when it is not being used for disk I/O. This "connection uses Pin 35 of the STD bus backplane, a signal normally assigned to IOEXP. To enable this option install jumper JB8.

3.7 DMA Priority Chain (JB9)

The STD-Z80 BUS was not originally designed to accommodate more than one DMA device. A problem could exist when two DMA controllers attempted to access the bus at the same time. dy-4 SYSTEMS has developed a technique whereby multiple DMA devices can operate in a prioritized fashion similar to the existing interrupt priority chain provided on the STD BUS.

dy-4 SYSTEMS backplanes incorporate a DMA priority daisy chain using the /BUSAK and /STATUS 0 signal lines (pins 41 and 40 respectively.) Effectively, the DMA device closest to the processor will get control of the bus if two or more are competing for it because it will receive the bus acknowledge signal, pre-

venting those cards further away from the processor from sensing it. If that card did not request the bus, the /BUSAK flows through to be recognized by the next highest DMA device.

Jumper block JB9 of the DSTD-777 allows this signal chain to be carried forward by shunting traces 40 and 41 on the bus. If not used with a dy-4 SYSTEMS backplane, this jumper block should be left open.

Note that even when the DSTD-777 is used in hardware DMA mode with the DSTD-711 it does not generate bus requests itself.

SECTION 4

4.0 SPECIFICATIONS

4.1 Electrical Specifications

4.1.1 Maximum System Clock

DSTD-777 4.0MHz + 0.05%

4.1.2 STD BUS Interface

Bus Inputs: One 74LS load max.

Bus Outputs: I_{OL} = 24 mA min. @ V_{OL} = 0.5 Volts
I_{OH} = 15 mA min. @ V_{OH} = 2.4 Volts

4.1.3 Operating Temperature

0 Degrees C to 50 Degrees C
95% humidity non-condensing

4.1.4 Power Supply Requirements

DSTD-777 5V +/- 5% @ 1.8A max
12V +/- 5% @ 100mA max

4.2 Mechanical Specifications

4.2.1 Card Dimensions

4.50 in. (11.43 cm.) wide by 6.50 in. (16.51 cm) long

0.48 in. (1.22 cm.) maximum height

0.062in.(0.16 cm.)printedcircuitboard thickness

4.2.2 STD Bus Edge Connector

56 pin Dual Readout; 0.125 in. centers

Mating Connector

Viking 3VH28/1CE5 (printed circuit)
Viking 3VH28/1CND5 (wire wrap)
Viking 3VH28/1CN5 (solder lug)

4.3 Software Specifications

I/O Map

base + 0	R/W	GDC Status Reg, GDC parameter FIFO write
base + 1	R/W	GDC FIFO Read, GDC command FIFO write
base + 2	R/O	bit 0 active Hi: DRQ from GDC this bit is read by S/W to determine when the GDC is ready for the next DMA access.
base + 3	R/W	DMA to/from GDC

Video Memory

There are 64K words of video memory on the DSTD-777. Address 0 bit 0 corresponds to the top left corner of the screen. A 'one' written into video memory will cause a pixel to turn off, and a 'zero' in video memory will cause a pixel to turn on.

For the DSTD-777A the 64K words are arranged as 3 pages; each page is 20480K words long. Page 0 is Red; Page 1 is green and Page 2 is blue. Hence to set the top left pixel to blue, address 0 bit 0 is set to 'one'; address 20480 bit 0 is set to 'one' and address 40560 bit 0 is set to 'zero'.

For the DSTD-777B there is only one page of video memory. Address 0 bit 0 is in the top left corner and Address 49151 bit 15 is the pixel at the bottom right corner.

SECTION 5

5.0 FACTORY NOTICES

5.1 FACTORY REPAIR SERVICE

In the event that difficulty is encountered with this unit, it may be returned directly to dy-4 for repair. This service will be provided free of charge if the unit is returned within the warranty period. However, units which have been modified or abused in any way will not be accepted for service, or will be repaired at the owner's expense.

When returning a circuit board, place it inside the conductive plastic bag in which it was delivered to protect the MOS devices from electrostatic discharge. **THE CIRCUIT BOARD MUST NEVER BE PLACED IN CONTACT WITH STYROFOAM MATERIAL.** Enclose a letter containing the following information:

Name, address and phone number of purchaser
Date and place of purchase
Brief description of the difficulty

Mail a copy of this letter **SEPARATELY** to the closest office:

dy-4 SYSTEMS INC.
888Lady Ellen Place
Ottawa, Ontario
K1Z 5M1, Canada

-or-

dy-4 SYSTEMS INC.
3582Dubarry Rd.
Indianapolis, IN 46226

Securely package and mail the circuit board, prepaid and insured, to the same address.

5.2 LIMITED WARRANTY

dy-4 warrants this product against defective materials and workmanship for a period of one year from date of purchase. This warranty does not apply to any product that has been subjected to misuse, accident, or improper installation, application, or operation, nor does it apply to any product that has been repaired or altered by other than our authorized factory representative.

There are no warranties which extend beyond those herein specifically given.

NOTICE

The antistatic bag is provided for shipment of dy-4 products to prevent damage to the components due to electrostatic discharge. Failure to use this bag in shipment will **VOID** the warranty.

APPENDIX A

OPTION JUMPER SUMMARY INCLUDING FACTORY SETTINGS

APPENDIX A

OPTION JUMPER SUMMARY

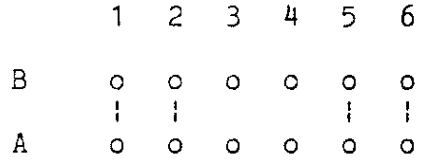
A - 1 Optional Jumper Blocks

The DSTD-777 has the following jumpers.

JB1	Card Address Selection
JB2	Output Driver Configuration Block
JB3	Output Driver 1 Configuration
JB4	On-board Pixel Clock Source
JB5	Separate/Composite Sync Select
JB6	Vertical Sync Source Selection
JB7	RAM Timing Selection
JB8	External DMA Chip Option
JB9	DMA Chain Option

A - 2 Card Address Selection (JB1)

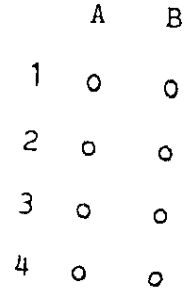
This jumper block sets the module's I/O address port.



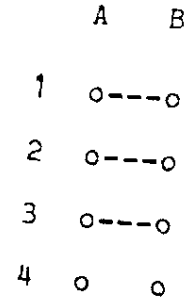
A1 to A8	Ground
B1	Address Bit 2
B2	Address Bit 3
B3	Address Bit 4
B4	Address Bit 5
B5	Address Bit 6
B6	Address Bit 7

A - 3 Output Driver Configuration Blank (JB2)

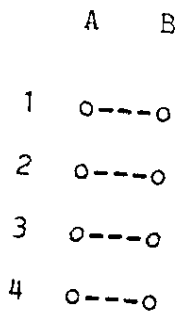
DSTD-777A (Color) w/separate sync



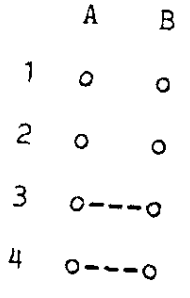
DSTD-777A (B/W) w/separate sync



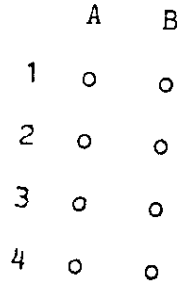
DSTD-777A (B/W) *w/comp sync* on video



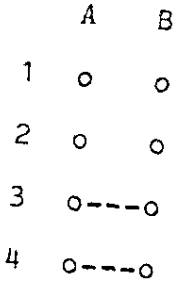
DSTD-777A (Color) w/sync on green



DSTD-777B w/separate sync



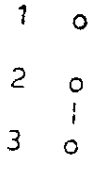
DSTD-777B *w/comp sync* on video



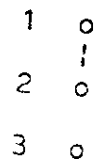
Pin 1A,2A,3A,4A O/P of Green Driver, *summing node for video* buffer
1B O/P of Red Driver
2B O/P of Blue Driver
3B I/P of Video Buffer
4B O/P of Composite Sync Driver

A - 4 Output Driver Configuration (JB3)

Configuration A



Configuration B



Set Configuration A for

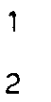
DSTD-777A Colour
DSTD-777B w/separate sync

Set Configuration B for

DSTD-777A B/W w/separate sync
DSTD-777A B/W w/composite sync on video
DSTD-777A Colour w/sync on green
DSTD-777B w/composite sync on video

Pin	1	O/P of Green Driver
	2	Pin 2 of J2
	3	O/P of Video Buffer

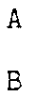
A - 5 On-board Pixel Clock Source (JB4)



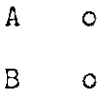
Pin	1	pin 12 of J2 and pixel clock of DSTD-777
	2	buffered pixel clock

A - 6 Separate / Composite Sync Select (JB5)

Composite Sync



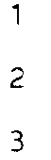
Separate Sync



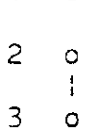
Pin A Set H sync
Pin B gnd.

A - 7 Vertical Sync Source Selection (JB6)

Extend Sync Mode



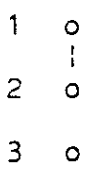
Master Sync Mode



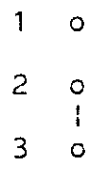
Pin	1	Vsync from NEC chip
	2	Pin 6 of J2
	3	Buffered Vsync

A - 8 RAM Timing Selection (JB7)

DSTD-777A

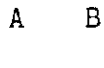


DSTD-777B



Pin	1	PCLK
	2	Clock for ROWSEL
	3	PCLK/2

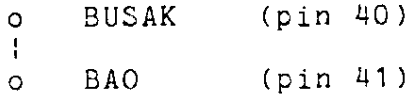
A - 9 External DMA Chip Option (JB8)



Pin	A	Pin 35 of STD backplane
Pin	B	Buffered Output of DRQ of GDC

A - 10 DMA Chain Option (JB9)

This jumper should be installed only when the card is used in a dy-4 SYSTEMS backplane.



APPENDIX B

STD-Z80 BUS PIN OUT

APPENDIX B

STD-Z80 BUS PIN OUT AND DESCRIPTION

BUS	MNEMONIC	DESCRIPTION
1	5V	5Vdc system power
2	5V	5Vdc system power
3	GND	Ground - System signal ground and DC return
4	GND	Ground - System signal ground and DC return
5	-5V	-5Vdc system power
6	-5V	-5Vdc system power
7	D3	
8	D7	
9	D2	Data Bus (Tri-state, input/output active high). D0-D7 constitute an 8-bit bidirectional data bus. The data bus is used for data exchange with memory and I/O devices
10	D6	
11	D1	
12	D5	
13	D0	
14	D4	
15	A7	
16	A15	
17	A6	Address Bus (Tri-state, output, active high).
18	A14	

19 20 21 22 23 24 25 26 27 28 29 30	A5 A13 A4 A12 A3 A11 A2 A10 A1 A9 A0 A8	A0-A15 make up a 16-bit address bus The address bus provides the address for memory (up to 65k bytes) data exchanges and for I/O device data exchanges. I/O addressing uses the lower 8 address bits to allow the user to directly select up to 256 input or 256 output ports. A0 is the least signficant address bit. During refresh time, the lower 7 bits contain a valid refresh address for dynamic memories in the system.
31	/WR	Memory Write (Tri-state, output, active low). /WR indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.
32	/RD	Memory Read (Tri-state, output, active low). /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.
33	/IORQ	Input/Output Request (Tri-state, output, active low). The /IORQ signal indicates that the lower half of the address bus holds a valid I/O address for an I/O read or write operation. An /IORQ signal is also generated with an /M1 signal when an interrupt is being acknowledged to indicate than an interrupt response vector can be placed on the data bus. Interrupt Acknowledge operations occur during /M1 time, while I/O operations never occur during /M1 time.
34	/MEMRQ	Memory Request (Tri-State output, active low). The /MEMRQ signal indicates that the address bus holds a valid address for a memory read or write operation.
35	/IOEXP	I/O expansion, not used on dy-4 Systems DSTD.

36	/MEMEX	Memory expansion, not used on dy-4 Systems DSTD cards.
37	/REFRESH	/REFRESH (Tri-state, output, active low). /REFRESH indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the /MEMRQ signal should be used to perform a refresh cycle for all dynamic RAMs in the system. During the refresh cycle A7 is a logic zero and the upper 8 bits of the address bus contains the I register.
38	/DEBUG	/DEBUG (Input) used in conjunction with DDT-80 operating system and the MDX Single Step card for implementing a hardware single step. When pulled low, the /DEBUG line will set a latch that will force the upper three address lines to a logic 1. To reset this latch, an I/O operation must be performed.
39	/M1	Machine Cycle One (Tri-state, output, active low). /M1 indicates that the current machine cycle is in the opcode fetch cycle of an instruction. Note that during the execution of a 2-byte opcodes, /M1 will be generated as each opcode is fetched. These two-byte op-codes always begin with a CBH, DDH, EDH or FDH. /M1 also occurs with /IORQ to indicate an interrupt acknowledge cycle.
40	STATUS 0	DMA priority chain input.
41	/BUSAK	Bus Acknowledge (Output, active low). Bus Acknowledge is used to indicate to the requesting device that the CPU address bus, data bus, and control bus signals have been set to their high impedance state and the external device can now control the bus.

42	/BUSRQ	Bus Request (Input, active low). The /BUSRQ signal is used to request the CPU address bus, data bus, and control signal bus to go to a high impedance state so that other devices can control those buses. When /BUSRQ is activated, the CPU will set these buses to a high impedance state as soon as the Current CPU machine cycle is terminated, and the Bus Acknowledge (/BUSAK) signal is activated.
43	/INTAK	Interrupt Acknowledge (Tri-state output, active low). The /INTAK signal indicates that an interrupt acknowledge cycle is in progress, and the interrupting device should place its response vector on the data bus.
44	/INTRQ	Interrupt Request (Input, active low). The Interrupt Request Signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop (IFF) is enabled and if the /BUSRQ signal is not active. When the CPU accepts the interrupt, an acknowledge signal (/IORQ during an /M1) is sent out at the beginning of the next instruction cycle.
45	/WAITRQ	WAIT REQUEST (Input, active low). Wait request indicates to the CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active. The signal allows memory or I/O devices of any speed to be synchronized to the CPU.

46	/NMIRQ	Non-Maskable Interrupt request (Input, negative edge triggered). The Non-Maskable Interrupt request has a high priority than /INTRQ and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop. /NMIRQ automatically forces the CPU to restart to location 0066H. The program counter is automatically saved in the external stack so that the user can return to the program that was interrupted. Note that continuous WAIT cycle can prevent the current instruction from ending, and that a /BUSRQ will over-ride a /NMIRQ.
47	/SYSRESET	System Reset (Output, active low). The System Reset line indicates that a reset has been generated from either an external reset or the power-on reset circuit. The system reset will occur only once per reset request and will be approximately 2 microseconds in duration. The system reset will also force the CPU program counter to zero, disable interrupts, set the I register to 00H, set the R register to 00H and set Interrupt Mode 0.
48	/PBRESET	Pushbutton Reset (Input, active low). The Pushbutton reset will *generate a debounced system reset.*
49	/CLOCK	Processor Clock (Output, active low). Single phase system clock.
50	CNTRL	Auxiliary Timing
51	PCO	Priority Chain Output (Output, active high.) This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.

52	PCI	Priority Chain In (Input, active high). This signal is used to form a priority interrupt daisy chain when more than one interrupt driven device is being used. A high level on this pin indicates that no other devices of higher priority are being serviced by a CPU interrupt service routine.
53	AUX GND	Auxiliary Ground (Bussed)
54	AUX GND	Auxiliary Ground (Bussed)
55	+12V	+12Vdc system power
56	-12V	-12Vdc system power

NOTES:

1. The reference to input and output of a given signal is made with respect to the CPU module.

APPENDIX C

DSTD-777 PARTS LIST

DSTD 777A PARTS LIST

DY4PART	QTY	DESCRIPTION	DESIGNATION
PT012074	1	74LS74 TTL-LS	U36
PT012164	1	74LS164 TTL-LS	U35
PT012166	3	74LS166 TTL-LS	U10,U19,U29
PT012245	1	74LS245 TTL-LS	U37
PT012283	1	74LS283 TTL-LS	U12
PT012373	1	74LS373 TTL-LS	U30
PT012374	4	74LS374 TTL-LS	U17,U18,U27,U28
PT012682	1	74LS682 TTL-LS	U38
PT013005	1	74S05 TTL-S	U42
PT013074	2	74S74 TTL-S	U32,U33
PT013163	1	74S163 TTL-S	U34
PT013299	1	74S299 TTL-S	U9
PT015042	1	NEC 72200-2	U31
PT016004	3	DS3648 INTERFACE	U2,U11,U20
PT022000	1	78M05VL VOLTAGE REGULATOR, TO-39 PACKAGE	Q2
PT031004	16	4164-15 64K RAM, 150 ns., 64K X 1	U3-U8,U13-U16,U21-U26
PT036002	1	PAL16L8	U39
PT036003	1	PAL16R8	U40
PT036004	1	PAL16R6	U41
PT041101	3	1/4 WATT, 100 OHM, 5% RESISTOR	R1,R2,R7
PT041102	1	1/4 WATT, 1K OHM, 5% RESISTOR	R19
PT041151	5	1/4 WATT, 150 OHM, 5% RESISTOR	R3,R6,R10,R13,R14
PT041470	3	1/4 WATT, 47 OHM, 5% RESISTOR	R15,R16,R17
PT042040	3	3386B-1-501 500 OHM POTENTIOMETER	R4,R8,R12
PT043016	1	10 PIN, 9 RESISTOR, 1K OHM, SIP RESISTOR NETWORK	RN1
PT053000	3	TAG10M25, 10uf, 25V TANTALUM CAPACITOR	C3,C4,C28
PT059000	28	.1uf 63V.(.2 LD. SP.)1R67104M.POLYESTER FILM CAPACITOR	C1,C2,C5-C27,C29-C31
PT061001	1	2N2222A TRANSISTOR	Q1
PT101012	1	K1116A 14.31818 MHZ CRYSTAL OSCILLATOR	U1
PT111073	1	9209-1 CARD EJECTOR WITH PINS	
PT111091	1	32018 HEATSINK (AAVID) OR 204CB (WAKEFIELD)	Q2
PT122003	1	CHD6960WIS 60 PIN DOUBLE ROW HEADER	JB1,JB2
PT122004	1	CHS6936WIS 36 PIN SINGLE ROW HEADER	JB3-JB9
PT123004	1	87516-3 14 PIN RIGHT ANGLE CONNECTOR (AMP ONLY)	J2
PT126016	16	640358-3 16 PIN I.C. SOCKET	U3-8,13-16,21-26
PT126020	3	640464-3 20 PIN I.C. SOCKET	U39,U40,U41
PT126040	1	640379-3 40 PIN I.C. SOCKET	U31
PT349001	1	DSTD 777 DY00490-H-A1-1W1	
PT711034	1	777 MANUAL	

APPENDIX C

DSTD 777B PARTS LIST

DY4PART	QTY	DESCRIPTION	DESIGNATION
PT012074	1	74LS74 TTL-LS	U36
PT012164	1	74LS164 TTL-LS	U35
PT012245	1	74LS245 TTL-LS	U37
PT012283	1	74LS283 TTL-LS	U12
PT012373	1	74LS373 TTL-LS	U30
PT012374	4	74LS374 TTL-LS	U17,U18,U27,U28
PT012682	1	74LS682 TTL-LS	U38
PT013005	1	74S05 TTL-S	U42
PT013074	2	74S74 TTL-S	U32,U33
PT013163	1	74S163 TTL-S	U34
PT013299	1	74S299 TTL-S	U9
PT015006	1	7220A LSI (CERAMIC ONLY AVAILABLE)	U31
PT016004	3	DS3648 INTERFACE	U2,U11,U20
PT022000	1	78M05VL VOLTAGE REGULATOR, TO-39 PACKAGE	Q2
PT031004	16	4164-15 64K RAM, 150 ns., 64K X 1	U3-U8,U13-U16,U21-U26
PT036002	1	PAL16L8	U39
PT036003	1	PAL16R8	U40
PT036004	1	PAL16R6	U41
PT041101	3	1/4 WATT, 100 OHM, 5% RESISTOR	R1,R2,R7
PT041102	1	1/4 WATT, 1K OHM, 5% RESISTOR	R18
PT041151	5	1/4 WATT, 150 OHM, 5% RESISTOR	R3,R6,R10,R13,R14
PT041470	3	1/4 WATT, 47 OHM, 5% RESISTOR	R15,R16,R17
PT042040	3	3386B-1-501 500 OHM POTENTIOMETER	R4,R8,R12
PT043016	1	10 PIN, 9 RESISTOR, 1K OHM, SIP RESISTOR NETWORK	RN1
PT053000	3	TAG10M25, 10uf, 25V TANTALUM CAPACITOR	C3,C4,C28
PT059000	28	.1uf 63V,(.2 LD. SP.)1R67104M.POLYESTER FILM CAPACITOR	C1,C2,C5-C27,C29-C31
PT061001	1	2N2222A TRANSISTOR	Q1
PT101013	1	LOCO II 31.22 MHZ CRYSTAL OSCILLATOR	U1
PT111073	1	9208-1 CARD EJECTOR WITH PINS	
PT111091	1	3201B HEATSINK (AAVID) OR 204CB (WAKEFIELD)	Q2
PT122003	1	CHD6960WIS 60 PIN DOUBLE ROW HEADER	JB1,JB2
PT122004	1	CHS6936WIS 36 PIN SINGLE ROW HEADER	JB3-JB9
PT123004	1	87516-3 14 PIN RIGHT ANGLE CONNECTOR (AMP ONLY)	J2
PT126016	16	640358-3 16 PIN I.C. SOCKET	U3-8,13-16,21-26
PT126020	3	640464-3 20 PIN I.C. SOCKET	U39,U40,U41
PT126040	1	640379-3 40 PIN I.C. SOCKET	U31
PT349001	1	DSTD 777 DY00490-H-A1-1W1	
PT711034	1	777 MANUAL	

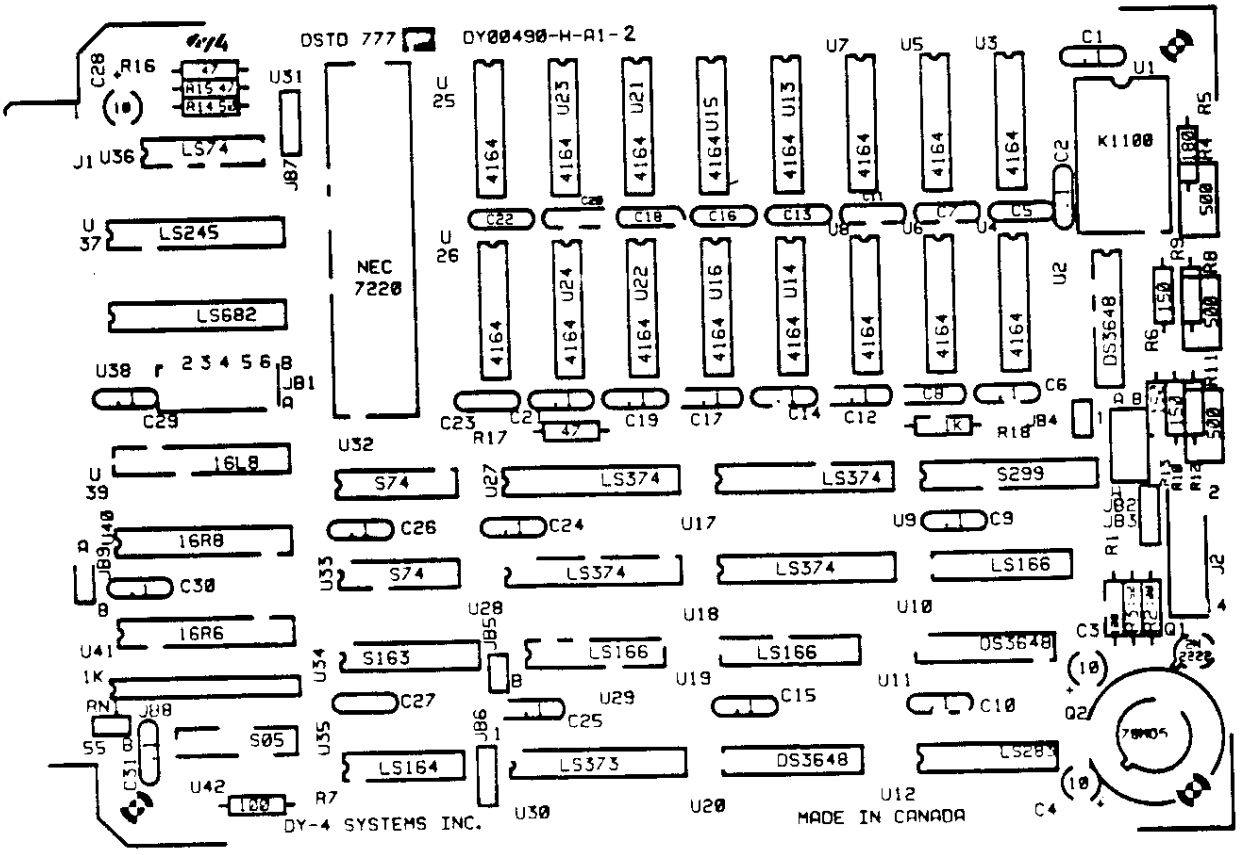
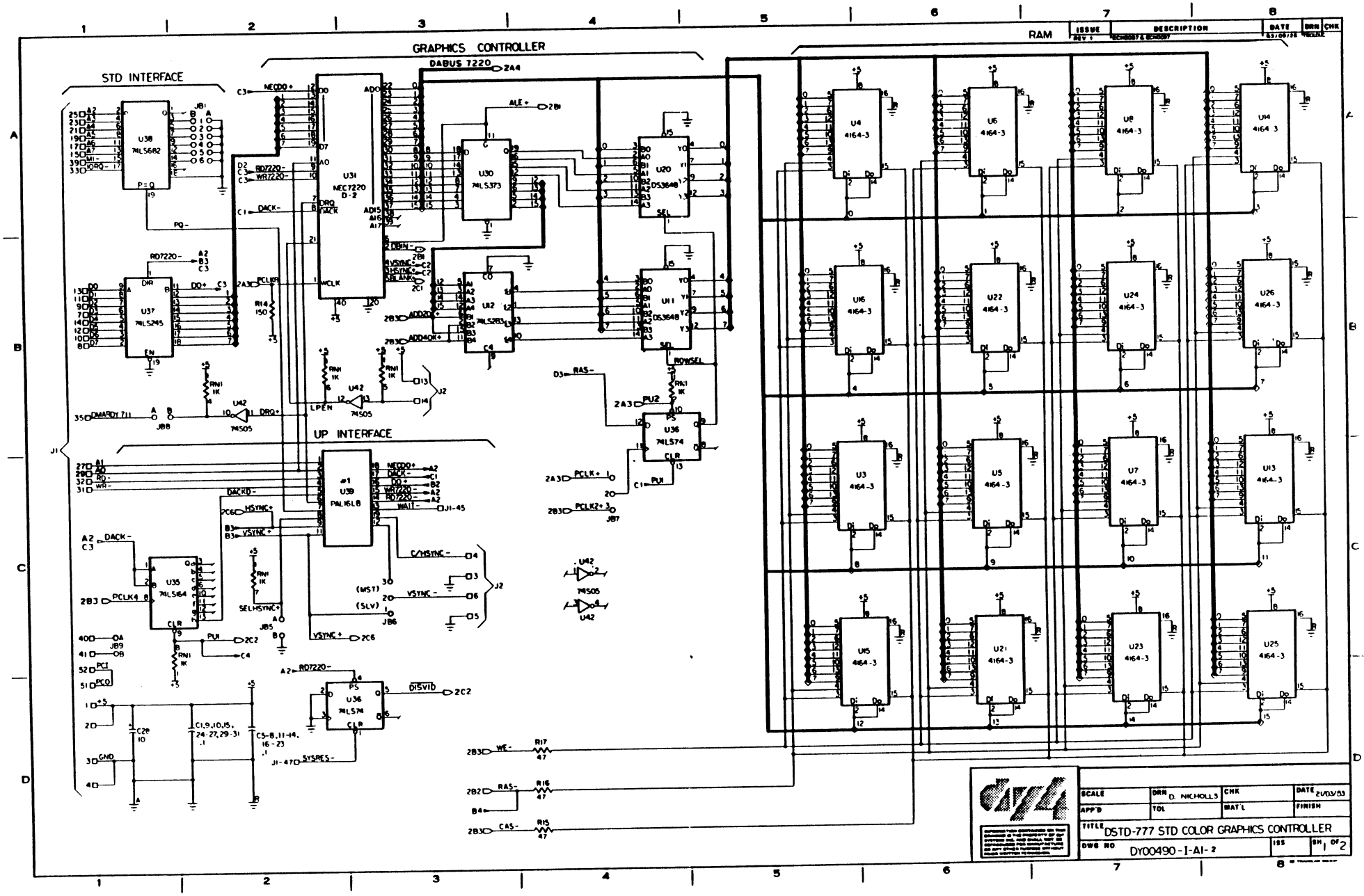
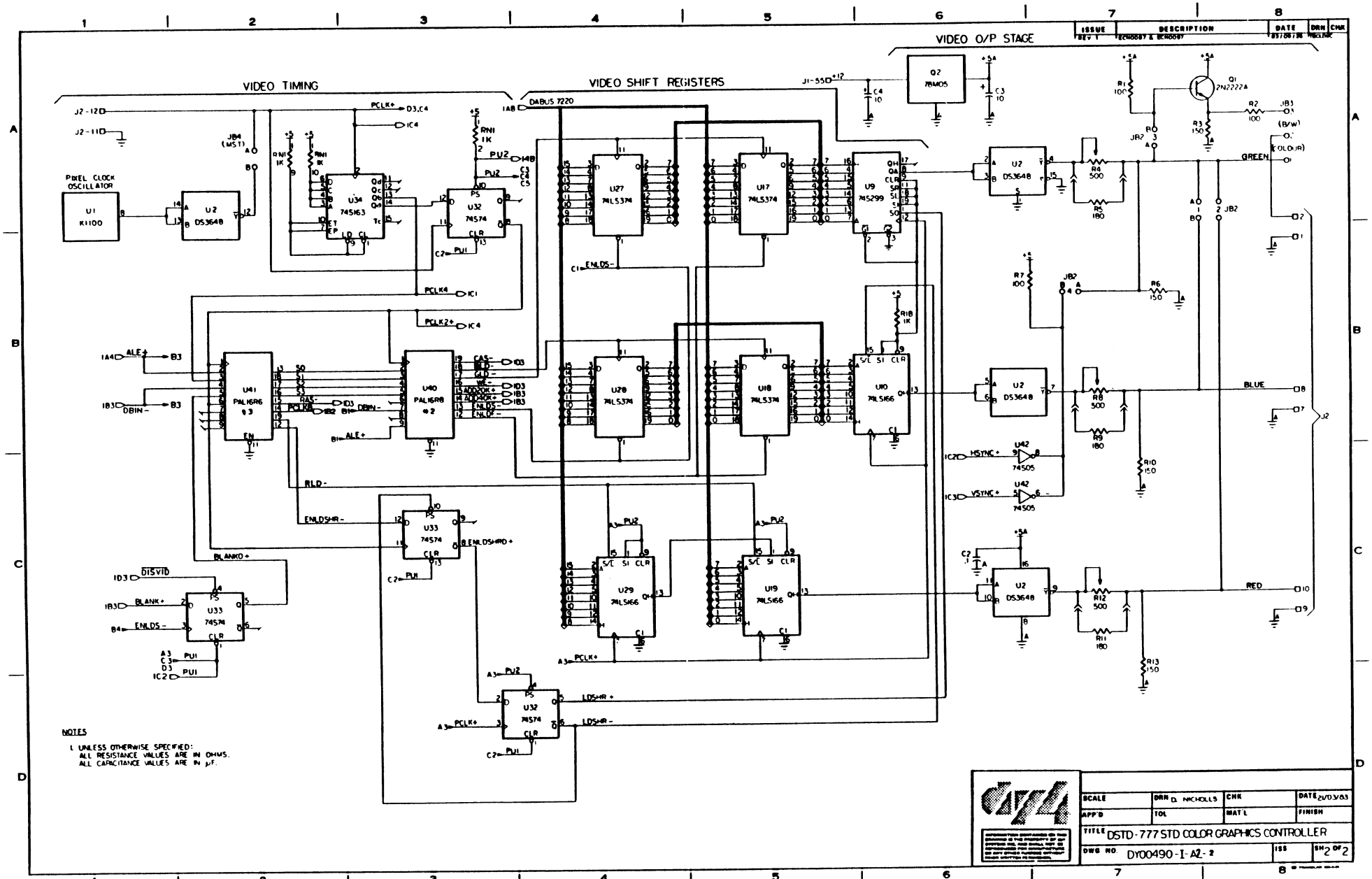


FIGURE C - 1 DSTD-777 SILK SCREEN

APPENDIX D

DSTD-777 SCHEMATIC


GRAPHICS CONTROLLER
STD INTERFACE
UP INTERFACE
RAM
DABUS 7220
U31 NEC7220 D-2
U38 74LS682
U37 74LS245
U30 74LS373
U20 DS3648
U11 DS3648
U12 74LS283
U36 74LS74
U39 PAL16L8
U35 74LS164
U42 74S05
U4 4164-3
U6 4164-3
U8 4164-3
U14 4164-3
U16 4164-3
U22 4164-3
U24 4164-3
U26 4164-3
U3 4164-3
U5 4164-3
U7 4164-3
U13 4164-3
U15 4164-3
U21 4164-3
U23 4164-3
U25 4164-3
DSTD-777 STD COLOR GRAPHICS CONTROLLER
DY00490-I-AI-2
D. NICHOLLS
2/03/83


VIDEO TIMING
VIDEO SHIFT REGISTERS
VIDEO O/P STAGE
ISSUE
DESCRIPTION
DATE
DRN
CHK
PIXEL CLOCK OSCILLATOR
U1 K1100
U2 DS3648
U34 74S163
U32 74S74
U27 74LS374
U17 74LS374
U9 74S299
U28 74LS374
U18 74LS374
U10 74LS166
U29 74LS166
U19 74LS166
U41 PAL16R6 #3
U40 PAL16R8 #2
U33 74S74
U42 74S05
Q2 78M05
Q1 2N2222A
DABUS 7220
PCLK+
PCLK4
PCLK2+
PU1
PU2
ALE+
DBIN-
RLD-
ENLDSHR-
BLANKO+
DISVID
BLANK+
ENLDS-
HSYNC+
VSYNC+
LDSHR+
LDSHR-
GREEN
BLUE
RED
(B/W)
(COLOUR)
NOTES
1. UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE VALUES ARE IN OHMS.
ALL CAPACITANCE VALUES ARE IN µF.
SCALE
DRN D. NICHOLLS
CHK
DATE 21/03/83
APP'D
TOL
MAT'L
FINISH
TITLE DSTD-777 STD COLOR GRAPHICS CONTROLLER
DWG NO. DY00490-I-A2-2
ISS
SH 2 OF 2